a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the first conductive type and provided on the channel region, wherein:

an impurity concentration in the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.

REMARKS

Claims 1, 4, 12 and 20-30 are pending. By this Amendment, claims 1, 4, 12, 22-23, 26 and 28-30 are amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise any new issue requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) do not present any additional claims without canceling a corresponding number of finally rejected claims; and (d) place the application in better form for appeal, should an appeal be necessary. Entry of the amendments is thus respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

Applicant gratefully acknowledge in item 4 of the Office Action indicating that claims 20 and 21 are allowed.

I. Rejection under 35 U.S.C. §112, First Paragraph

The Office Action rejects claims 4, 12 and 22-30 under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification. This rejection is respectfully traversed.

Specifically, with respect to claim 4, the first conductive type means p+-type source region 21 in the specification. The p+-type source region 21 is provided between n drift region 14 (which functions as a n channel region) and the source electrode 22. Claim 4 is now amended to clarified the terms.

Likewise, claims 12, 22-23, 26, 28-29 and 30 have been amended for clarity of the semiconductor structure as disclosed in this specification.

Accordingly, withdrawal of the rejection of claims 4, 12 and 22-30 under 35 U.S.C. §112, first paragraph, as containing subject matter not disclosed in the specification is respectfully solicited.

II. Rejection under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 1 and 4 under 35 U.S.C. §112, second paragraph, as being indefinite. In response, the claims are amended above to obviate the rejection. Withdrawal of the rejection of claims 1 and 4 under 35 U.S.C. §112, second paragraph, as being indefinite is respectfully requested.

III. Conclusion

For at least the reason discussed above, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Richard J. Kim
Registration No. 48,360

JAO:RJK/sld

Attachment:
Appendix

Date: April 18, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (~~Twice~~ Three Times Amended) A bipolar semiconductor device comprising:

a drain electrode;

a drain region ~~formed of a p+ type semiconductor~~having a first conductive type and disposed on the drain electrode;

a drift region having a second conductive type different from the first conductive type of the drain region and disposed on the drain region;

a channel region having the second conductive type and disposed on the drift region;

a gate region surrounding at least a part of the channel region via an insulation film, the gate region ~~formed of a p+ type semiconductor~~having the first conductive type;

a source region having the second conductive type provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film; and

a source electrode connected to the source region,

wherein a depletion layer is formed over most of the entire channel region when a predetermined voltage is applied to the gate region.

4. (Twice Amended) The semiconductor device according to claim 1, further comprising a semiconductor region ~~formed of a p+ type semiconductor~~having the first conductive type and provided between the channel region and the source ~~region~~electrode.

12. (~~Three~~ Four Times Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a second conductive type different from the first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the ~~second~~ first conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film, wherein:

an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.

22. (Amended) The semiconductor device according to claim 12, wherein:

the gate region has the first conductive type~~; and~~.

~~a depletion region is formed over most of the entire channel region when a predetermined voltage is applied to the gate region.~~

23. (Amended) The semiconductor device according to claim 22, further comprising ~~a semiconductor region having the first conductive type disposed between the channel region and the source electrode~~a source electrode provided on the source region.

26. (Amended) The semiconductor device according to claim 12, further comprising a semiconductor layer having the ~~second~~ first conductive type located between the source region and the source electrode, the semiconductor layer including an end face extended to a position covering at least a portion of the gate region.

28. (Amended) The semiconductor device according to claim 26, further comprising an insulation ~~film~~ layer located between the semiconductor layer and the source electrode and having an opening portion for the semiconductor layer and the source electrode to contact, wherein a width of the opening portion is wider than a distance of the gate region.

29. (Amended) The semiconductor device according to claim 27, further comprising an insulation ~~film~~ layer located between the ~~conductive~~ semiconductor layer and the source electrode, and having an opening portion for the semiconductor layer and the source electrode to contact, wherein a width of the opening portion is wider than a space of the gate region.

30. (Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having ~~a second~~the first conductive type ~~different from the first conductive type, the source region being~~ and provided on the channel region ~~and located substantially at a center of the channel region, and the source region being isolated from the insulation film~~, wherein:

~~wherein~~ an impurity concentration ~~of~~ in the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.